REMARKS

The above amendments and following remarks are submitted in response to the Official Action of the Examiner mailed May 10, 2005. Having addressed all objections and grounds of rejection, claims 1-25, being all the pending claims, are now deemed in condition for allowance. Reconsideration to that end is respectfully requested.

Applicants wish to thank the Examiner for his reminder of the continuing duty of candor under 37 C.F.R. 1.56. However, the Examiner has perhaps made an unintentionally burdensome request stating:

> The Examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. (Emphasis added)

As the Examiner is no doubt aware, this includes all U.S. Patents having a filing date prior to the filing date of the subject application. Fully over six million references are included within this category. Furthermore, the number of U.S. Patents is dwarfed by the number of non-patent documents which have been generated over 6,000 years of recorded history. Surely, the Examiner wishes Applicants to cite only pertinent prior art.

In this regard, shortly after the filing date of the subject application on December 12, 2000, Applicants filed an Information Disclosure Statement. Of the references cited therein, those

deemed most pertinent have already been discussed in Applicants' Background of the Invention section of the subject patent application. Of course, the Inventors and others associated with the preparation and prosecution of this patent application acknowledge their continuing duty in this regard. However, because it is nearly five (5) years since the filing of this application, it is becoming quite unlikely that more pertinent prior art will come to the attention of anyone associated with this prosecution in the normal conduct of business. Nevertheless, Applicants wish to express their gratitude for this reminder.

Claims 11-15 have been rejected under 35 U.S.C. 112, first paragraph. In response thereto, claim 11 has been amended to remove the language indicated by the Examiner as not supported in the specification.

Claim 16 has been rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,564,035, issued to Lai (hereinafter referred to as "Lai"). This rejection is respectfully traversed as to amended claim 16 for the following reasons.

Claim 16 has been amended to require that the level one caching means is "semi-store-through" and that the level two caching means is dedicated to the claimed "executing means". These limitations are fully supported in the specification and

are summarized at page 6, line 21, through page 7, line 7. The rejection of claim 16, and all claims depending therefrom, is respectfully traversed.

Claim 1 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (hereinafter referred to as "AAPA") in view of Lai. This ground of rejection is respectfully traversed as to amended claim 1 for the following reasons.

Claim 1, as amended, no longer comports with 37 C.F.R. 1.75(e) as a "Jepson" style claim. As amended, claim 1 is now an independent apparatus claim having four basic elements. Lai does not show the claimed combination of these elements.

Claim 1 has also been amended to specifically recite invalidation "in response to a SNOOP hit from a write request by another processor". This limitation is described in detail in the specification at page 14, lines 9-17. Motivation for this amendment is found in the Examiner's findings in paragraph 5(e) of the pending official action. It is assumed that the Examiner admits that the prior art of record does not show this limitation.

The rejection of amended claim 1, and all claims depending therefrom, is respectfully traversed.

Claims 2-4 have been rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lai and further in view

of U.S. Patent No. 6,061,766, issued to Lynch et al (hereinafter referred to as "Lynch"). This ground of rejection is respectfully traversed for the reasons provided below.

Applicants have provided substantial previous arguments concerning the lack of showing of motivation and lack of showing of reasonable likelihood of success of the alleged combination as required by MPEP 2143.

Furthermore, claims 2-4 depend from claim 1, which is deemed patentable for the reasons provided above. Claims 2-4 are each limited by unique limitation which have been discussed at length in previous responses. For example, claim 2 is limited by "second logic" which inhibits invalidation under certain conditions. This is not found in the prior art of record. The rejection of amended claim 2 is respectfully traversed.

Similarly, claim 3 requires a "third logic" which is not found in the prior art of record. Instead, the Examiner makes a finding of inherency stating:

> It is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed for follow; clearly the use of multiple logics is an inherent feature of any computer system.

This finding does not comport with the requirements of MPEP 2112 for number of reasons. Most importantly, however, the Examiner does not address the claimed "data processing system" but relies upon assumed features of "any computer system", which is not

claimed. The rejection of amended claim 3 is respectfully traversed.

Claim 4 is further limited by "fourth logic which records location of data in response to a level one cache memory read miss and a level two cache memory read miss". As with Applicants, the Examiner is apparently unable to find this limitation within the prior art of record. Therefore, instead of addressing the claimed invention, the Examiner simply ignores the obligation of MPEP 2143 to show "all claimed elements" within the alleged combination and finds the claim obvious. The rejection of claim 4 is respectfully traversed.

Claim 5 has been rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lynch and further in view of Lai and further in view of U.S. Patent No. 4,891,809, issued to Hazawa (hereinafter referred to as "Hazawa"). This ground of rejection is respectfully traversed for the following reasons.

Claim 5 depends from claim 3 and is further limited by a "Fifth logic which detects a parity error in said level two cache memory and which in response invalidates said corresponding level one cache memory location[1] to avoid loss of control between said level one cache memory and said level two cache memory". In other words, the claimed "fifth logic" detects and invalidates a

[1]The Examiner never uses the term "memory location" in his rejection leading one to suspect that he has confused the claimed single memory location with the entire memory. The practical significance of this distinction should be readily apparent.

memory location in response thereto. In making his rejection, the Examiner cites Hazawa column 3, lines 38-49, which does not detect but generates a "pseudo-error" in accordance with column 3, line 26. Furthermore, the most that Hazawa can do about such a "pseudo-error" (or perhaps even an actual parity error) is set one of "error indicating flags" 45, 46, 47, or 48. None of these "error indicating flags" can specify the location of an error, but can only indicate that an error has occurred (i.e., been generated as a "pseudo-error") somewhere in the memory. The alleged combination cannot meet the limitations of claim 5. The rejection of claim 5 is respectfully traversed.

Claims 6 and 9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lai and further in view of U.S. Patent No. 6, 128,711. This ground of rejection is respectfully traversed.

Claim 6 has six individual major elements. The alleged combination does not have all of these major elements and in particular does not have either element e. or element f. The rejection of claim 6, and all claims depending therefrom, is respectfully traversed.

Claim 9 depends from claim 6 and is further limited by a "fourth logic" which performs the recording of an invalidated location. The alleged combination has no such element. The rejection of claim 9 is respectfully traversed.

Claims 7 and 8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lai and further in view of Duncan and further in view of Lynch. This ground of rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness as required by MPEP 2143.

Claim 10 has been rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, in view of Lai, further in view of Duncan, and further in view of Hazawa. This ground of rejection is respectfully traversed.

In addition to the issues raised above concerning the claim from which claim 10 depends, the alleged combination does not have circuitry which invalidates a "corresponding portion" of the level one cache memory. In fact, the Examiner does not even consider the claimed elements. Instead, he states:

> Hazawa discloses invalidating a level one cache memory in response to a level two cache memory generating a parity error (col. 3, lines 38-48).

This finding is clearly erroneous, because Hazawa shows only generation of a "pseudo-error" by Diagnostic Unit 1. There is no parity error generated by Cache Memory Unit 2. The Examiner's statement is also legally irrelevant, because it does not address the claimed invention. The Examiner discusses invalidating the entire level one cache memory. This is not claimed. The rejection of claim 10 is respectfully traversed.

Claims 11 and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Duncan. This ground of rejection is respectfully traversed as to the amended claims.

Claim 11 is a method claim having four basic steps. It requires an environment having a "semi-store-through level one cache memory". This element is important to the operation of the method. Neither Lai nor Duncan nor any of the other prior art of record has the claimed "semi-store-through level one cache memory". Therefore, the rejection of claim 11, and all claims depending therefrom, is respectfully traversed.

Claim 14, as amended, depends from claim 11 and is limited by three additional steps including "recording location of data corresponding to said read memory request within said level one cache memory" wherein the record of location of the data must be made within the level one cache memory. Neither Lai nor Duncan nor any of the prior art of record meets this limitation. Therefore, in making his rejection, the Examiner cites column 6, line 65, through column 7, line 11, of Lai alleging the recording of the location of the data. This is not responsive to the claimed invention. The rejection of claim 14 is respectfully traversed.

Claims 12-13 and 17-18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Lynch. This

ground of rejection is respectfully traversed for the reasons discussed below.

Each of these claims depend from either amended claim 11 or amended claim 16 which are deemed patentable over the alleged rejection as anticipated by Lai for the reasons presented above. The embodiment of Lai relied upon by the Examiner for his rejection of claims 11 and 16 is the fully inclusive prior art example shown at Fig. 3 of Lai. One would not combine that embodiment with Lynch to add the claimed limitations of claims 12-13 and 17-18 because such additions would be superfluous. Lai has no mode 3 with ownership, because this would make no sense in the applied architecture of Lai which employs full inclusion of level one cache memory in level two cache memory. The Examiner continues to mix architectures in ways which do not make any sense. Similarly, Lai has no need for the claimed elements of claims 13 and 18. The fully inclusive architecture chosen by the Examiner does not and cannot utilize these elements. The rejection of claims 12-13 and 17-18 is respectfully traversed.

Claims 15 and 20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Hazawa. This ground of rejection is respectfully traversed for the reasons provided below.

Both claims 15 and 20 require detection of a parity error. Hazawa only shows generation of a "pseudo-error". There is no

disclosure of an actual parity error or structure in response thereto. Furthermore, claim 15 requires invalidation of a "portion" of the data, whereas claim 20 requires invalidation of an "element". Hazawa does not invalidate any particular portion or element. It simply sets a flag with regard to the entire cache memory. With Hazawa, one cannot distinguish between whether there is a single byte containing a parity error or whether the entire cache memory is inoperative. The rejection of claims 15 and 20 is respectfully traversed.

Claim 21 has been rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Hazawa. This ground of rejection is respectfully traversed.

Claim 21 requires "a data element having a parity error stored in said level two cache memory" and "a facility which detects said parity error of said data element and invalidates a corresponding data element within said level two cache memory". The alleged combination does not have these elements. Perhaps acknowledging this lack of teaching, the Examiner states:

> Hazawa discloses invalidating data in a level two cache memory in response to a parity error of a data element to provide a cache memory with an error checking mode [col. 3, lines 38-51; col. 3, lines 38-59].

This statement ignores both the clear language of Applicants' claims and the clear teaching of Hazawa. Hazawa shows no "data element having a parity error" and no invalidation of a "corresponding data element". Furthermore, the claim requires

invalidation of a single data element. Hazawa has no way to determine the location of any particular parity error. The rejection of claim 21 is respectfully traversed.

Claim 22 has been rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, in view of Hazawa, and further in view of Lynch. This ground of rejection is respectfully traversed.

In addition to the issues raised with regard to claim 21 from which claim 22 depends, the alleged combination does not have the additional claim elements. Therefore, the rejection of claim 22 is respectfully traversed.

Claims 23-25 have been rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, in view of Hazawa, in view of Lynch, and further in view of Lai. This ground of rejection is respectfully traversed because the Examiner has again alleged the combination of incompatible architectures for the purpose of adding superfluous functionality as explained in detail above. The rejection of claims 23-25 is respectfully traversed.

Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-25, being the only pending claims.

Please charge any deficiencies or credit any overpayment to Deposit Account No. 14-0620.

Respectfully submitted,

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By his attorney,

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